

PTO/SB/97 (08-03)

Approved for use through 07/31/2008. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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Beth Barnhart
Signature

Beth Barnhart

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* *Marietta, per our telecon on January 16, 2007 at 9:30 a.m., attached please find a Request for Certificate of Correction previously faxed to Valerie Jackson on September 12, 2006. Our requests for a Certificate of Correction date back to July 22, 2005. Your assistance in expediting this matter will be appreciated. Kindly telephone Beth Barnhart at 704-945-6720 to confirm receipt of this fax/request. Thank you.* *

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RE: US Patent 6,903,446 - Issued 7/6/2005 - Application Serial No. 10/045,766

September 12, 2006 Fax Cover Page and Fax Confirmation	2 pages
Request for Issue of Corrected Patent Transmittal Letter	2 pages
PTO/SB/44 Certificates of Correction	3 pages

TOTAL PAGES IN TRANSMISSION including PTO/SB/97 8 PAGES

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(703) 308-9390 X114
on September 12, 2006 Date Fax No. 571-270-9928



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(704) 945-6720

Beth Barnhart

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RE: US Patent 6,903,446 - Issued 7/6/2005 - Application Serial No. 10/045,766

Transmittal Letter 2 pages

PTO/SB/44 Certificates of Correction 3 pages

TOTAL PAGES IN TRANSMISSION including PTO/SB/97 6 PAGES

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on September 12, 2006

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No. : 10/045,766 Confirmation No: 3061
Applicant : Ralph C. Tuttle, *et al.*
Filed : 10/23/2001
TC/A.U. : 2811
Examiner : Andre C. Stevenson
Docket No. : 5000.142
Customer No. : 021176
For : PATTERN FOR IMPROVED VISUAL INSPECTION
OF SEMICONDUCTOR DEVICES

September 12, 2006

Certificate of Corrections Branch
Commissioner for Patents
Post Office Box 1450
Alexandria, VA 22313-1450

REQUEST FOR ISSUE OF CORRECTED PATENT

Sir:

Pursuant to 37 CFR §1.322(b), the Assignee of U.S. Patent No. 6,903,446 requests that the U.S. Patent and Trademark Office (PTO) issue a corrected patent in lieu of and with like effect as a certificate of correction with respect to the above-referenced patent. A brief explanation is listed hereafter and was previously submitted on July 22, 2005.

1. May 5, 2004 — Applicants file an Amendment and Reply to Office Action submitting that Claims 1, 4, 5, 10, 11, 14-17, 19, 20, and 27 are in condition for allowance.
2. August 25, 2004 — Examiner Stevenson mails a Notice of Allowability in response to the May 5, 2004, Amendment and Reply. Claims 10 and 27 are omitted.
3. October 13, 2004 — Applicant's attorney telephones Examiner Stevenson regarding the omitted claims. Examiner Stevenson states that he will call back if there is a reason the claims were not allowed. Otherwise, he will issue a Supplemental Notice of Allowability.
4. October 19, 2004 — Examiner Stevenson issues a Supplemental Notice of Allowability including Claims 10 and 27.

Certificate of Corrections Branch
Commissioner for Patents
Page 2

Confirmation No. 3061
US Patent 6,903,446

5. November 23, 2004 — Issue Fee paid.

6. June 7, 2005 — Patent No. 6,903,446 issues omitting the allowed subject matter claimed in Claims 10 and 27 (as amended in the May 5, 2004, Amendment and Reply to Office Action).

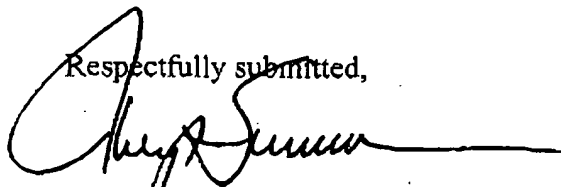
7. July 22, 2005 — Applicants file a Request for Issue of Corrected Patent with a summary of items 1-6 above featured on Certificate of Correction form PTO/SB/44.

8. June 19, 2006 and August 31, 2006 — Applicants submit Status Inquiries regarding the July 22, 2005 Request for Issue of Corrected Patent.

9. September 6, 2006 — Valerie Jackson of the Patent Publications Office contacts the Applicants' representative and requests that Applicants submit the attached Certificate of Correction form PTO/SB/44 containing all the claims as they should appear in the patent.

Accordingly, Form PTO/SB/44 is attached and the Applicants request that the PTO issue a corrected patent listing original and amended (per the May 5, 2004, Amendment and Reply) Claims 1, 4, 5, 10, 11, 14-17, 19, 20, and 27. Because the PTO is at fault in this matter, no fee is enclosed.

Respectfully submitted,



Philip Summa
Registration No. 31,573

Enclosures

PTO/SB/44 (04-05)

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(Also Form PTO-1050)

**UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION**Page 1 of 3

PATENT NO. : 6,903,446 B2

APPLICATION NO.: 10/045,766

ISSUE DATE : June 7, 2005

INVENTOR(S) : Ralph C. Tuttle, Christopher Sean Plunket, David B. Slater, Jr., Gerald H. Negley,
Thomas P. Schneider

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

That which is claimed is:

1. A labeled semiconductor material comprising:
a surface of silicon carbide; and
a first metal layer on portions but not all of said surface;
said metal layer forming a pattern with rotational symmetry of C_n , where n is at least 2.
2. A labeled semiconductor material comprising:
a surface of silicon carbide; and
a first metal layer on portions but not all of said surface;
said metal layer forming a pattern with rotational symmetry of C_n where n is at least 2;
a second metal layer on portions but not all of said surface of said semiconductor material;
said second metal layer forming a pattern different from said first metal layer pattern;
said second pattern having rotational symmetry of C_n where n is at least 2; and wherein each of said first and second patterns forms an X pattern.
3. A labeled semiconductor material comprising:
a surface of silicon carbide; and
a first metal layer on portions but not all of said surface;
said metal layer forming a pattern with rotational symmetry of C_n , where n is at least 2;
a second metal layer on portions but not all of said surface of said semiconductor material;
said second metal layer forming a pattern different from said first metal layer pattern;
said second pattern having rotational symmetry of C_n where n is at least 2;
wherein each of said first and second patterns forms an X pattern; and
wherein each X pattern further comprises a tab portion perpendicular to at least one of the arms of said X pattern.
4. A labeled semiconductor material according to claim 1 wherein said metal layer is selected from the group consisting of nickel, titanium, gold, platinum, vanadium, aluminum, alloys thereof and layered combinations thereof.

MAILING ADDRESS OF SENDER (Please do not use customer number below):

Summa, Allan & Additon, P.A.
11610 N. Community House Road, Suite 200
Charlotte, NC 28277

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PTO/SB/44 (04-03)

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UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

Page 2 of 3

PATENT NO. : 6,903,446 B2

APPLICATION NO.: 10/045,766

ISSUE DATE : June 7, 2005

INVENTOR(S) : Ralph C. Tuttle, Christopher Sean Plunket, David B. Slater, Jr., Gerald H. Negley,
Thomas P. Schneider

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

5. A semiconductor structure comprising:
a substrate having at least one planar face;
a first metal layer on said planar face, and covering some, but not all of said planar face in a first predetermined geometric pattern;
a second metal layer on said planar face, and covering some, but not all of said planar face in a second geometric pattern that is different from said first geometric pattern; and
an epitaxial layer on the opposite side of said substrate from said planar face and said metal layers.

6. A semiconductor structure comprising:
a substrate having at least one planar face;
a first metal layer on said planar face, and covering some, but not all of said planar face in a first predetermined geometric pattern;
a second metal layer on said planar face, and covering some, but not all of said planar face in a second geometric pattern that is different from said first geometric pattern; and
an epitaxial layer on the opposite side of said substrate from said planar face and said metal layers;
wherein said substrate and said epitaxial layer comprise a semiconductor device.

7. A semiconductor structure according to claim 6 wherein said device is selected from the group consisting of junction diodes, bipolar transistors, thyristors, MESFETS, JFETS, MOSFETs and photodetectors.

8. A semiconductor structure comprising:
a substrate having at least one planar face;
a first metal layer on said planar face, and covering some, but not all of said planar face in a first predetermined geometric pattern;
a second metal layer on said planar face, and covering some, but not all of said planar face in a second geometric pattern that is different from said first geometric pattern; and
an epitaxial layer on the opposite side of said substrate from said planar face and said metal layers;
wherein said substrate and said epitaxial layer comprise a semiconductor device; and
wherein said metal layers form an ohmic contact to said device.

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11610 N. Community House Road, Suite 200
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PTO/SB/44 (04-05)

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**UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION**Page 3 of 3

PATENT NO. : 6,903,446 B2

APPLICATION NO.: 10/045,766

ISSUE DATE : June 7, 2005

INVENTOR(S) : Ralph C. Tuttle, Christopher Sean Plunket, David B. Slater, Jr., Gerald H. Negley,
Thomas P. Schneider

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

9. A semiconductor structure according to claim 8 wherein said substrate and said epitaxial layer are silicon carbide and said metal layers are selected from the group consisting of nickel, titanium, gold, alloys thereof, and layered combinations thereof.

10. A semiconductor device according to claim 8 wherein said device comprises a light emitting diode or laser diode that includes a p-n junction, and with said ohmic contact comprising a layer of nickel on said substrate and a layer selected from the group consisting of titanium-gold alloys and titanium-platinum-gold alloys on said nickel layer.

11. A semiconductor wafer comprising:
a silicon carbide substrate and at least one silicon carbide epitaxial layer;
respective primary and secondary orthogonal flats;
respective front and back planar faces;
a plurality of devices on said wafer;
each said device having a first metal layer on said planar face, and covering some, but not all of said planar face in a first predetermined geometric pattern; and
each said device having a second metal layer on said planar face, and covering some, but not all of said planar face in a second geometric pattern that is different from said first geometric pattern.

12. A semiconductor wafer according to Claim 11 wherein:
said devices comprise light emitting diodes or laser diodes that include a p-n junction; and
said metal layers comprise a layer of nickel on said substrate and a layer of a titanium- gold alloy on said nickel layer that form respective ohmic contacts to said devices.

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